THAT WHICH IS CLAIMED IS:

1. An integrated circuit device, comprising:

a segmented CAM array that is configured to support a long word search operation as a plurality of overlapping segment-to-segment search operations that are each performed across different rows within a group of rows in the CAM array and staggered in time relative to one another.

2. The device of Claim 1, wherein the plurality of overlapping segment-to-segment search operations includes a first segment-to-segment search operation that is performed in a first row in the group of rows and a second segment-to-segment search operation that is performed a second row in the group of rows; and wherein commencement of the second segment-to-segment search operation is delayed in time relative to commencement of the first segment-to-segment search operation by one or two search segment time intervals.

3. The device of Claim 2, wherein upon commencement of the second segment-to-segment search operation, a precharged first match line segment in the first row is discharged in response to a leading edge of a force-to-miss control signal.

4. The device of Claim 2, wherein the second segment-to-segment search operation is preceded by the step of precharging a first match line segment in the second row while simultaneously discharging a corresponding first match line segment in the first row.

5. The device of Claim 1, wherein a first row within the group of rows comprises:

first and second match line segments; and

a match line driver that is electrically coupled to the first match line segment and is responsive force-to-miss control signal.

6. The device of Claim 5, wherein the first row further comprises:

a match line signal repeater having an input electrically connected to the first match line segment and an output electrically connected to the second match line segment.

7. The device of Claim 5, wherein the first row further comprises:

a dual-capture match line signal repeater having an input electrically connected to the first match line segment and an output electrically connected to the second match line segment.

8. The device of Claim 5, wherein said match line driver is configured to electrically short the first match line segment to a ground reference potential in response to a leading edge of the force-to-miss control signal.

9. The device of Claim 8, wherein said match line driver is configured to precharge the first match line segment in response to a trailing edge of an evaluation control signal.

10. An integrated circuit device, comprising:

a CAM array block having a segmented xN CAM array therein that is configured to support one-half of a x8N search operation as four overlapping segment-to-segment search operations that are performed in a staggered sequence across different rows within a quad group of rows in the CAM array.

11. The device of Claim 10, wherein a first one of the quad group of rows comprises:

a first segment of CAM cells;

a first match line segment that is electrically connected to the first segment of CAM cells; and

a match line driver that is electrically connected to said first match line segment, said match line driver configured to precharge said first match line segment in response to an edge of a control signal and discharge said first match line segment in response to an edge of a force-to-miss control signal.

12. The device of Claim 10, wherein each of the rows in the quad group is responsive to a respective force-to-miss control signal.

13. An integrated circuit device, comprising:

a CAM array having a segmented row of CAM cells therein that comprises:

first and second segments of CAM cells;

first and second match line segments that are electrically connected to said first and second segments of CAM cells, respectively;

a match line driver that is configured to precharge said first match line segment in response to an edge of a control signal and is responsive to a force-to-miss control signal; and

a dual-capture match line signal repeater having an input that is electrically coupled to said first match line segment and an output that is electrically coupled to said second match line segment.

14. The device of Claim 13, wherein said match line driver is configured to discharge said first match line segment in response to a leading edge of the force-to-miss control signal.

15. An integrated circuit device, comprising:

a CAM array having a row of CAM cells therein that comprises first and second local word line drivers, which are responsive to first and second local word line control signals, respectively, and first and second segments of CAM cells that are electrically coupled to the first and second local word line drivers, respectively.

16. The device of Claim 15, wherein the first and second local word line drivers are responsive to a global word line control signal.

17. The device of Claim 16, wherein said CAM array has another row of CAM cells therein that comprises third and fourth local word line drivers, which are responsive to third and fourth local word line control signals, respectively, and third and fourth segments of CAM cells that are electrically coupled to the third and fourth word line drivers, respectively; and wherein the third and fourth local word line drivers are responsive to the same global word line control signal as the first and second local word line drivers.

18. An integrated circuit device, comprising:

a CAM array having a row of lateral XY TCAM cells therein that are arranged in a repeating low-even, low-odd, high-even, high-odd sequence or a repeating high-even, high-odd, low-even, low-odd sequence.

19. An integrated circuit device, comprising:

a segmented CAM array that is configured to support pipelined long word search operations in segment-to-segment and row-to-row search directions using a plurality of force-to-miss control signals to identify which rows are to be searched in the row-to-row pipeline direction.

20. A method of operating an integrated circuit device, comprising the step of:

staggering the timing of overlapping segment-to-segment search operations across different rows within a CAM array using force-to-miss control signals to establish miss conditions on match lines of rows that are not participating in respective ones of the segment-to-segment search operations.

21. A content addressable memory (CAM) array, comprising:

a row of CAM cells having at least xR and xS segments of CAM cells therein that include xR and xS match line segments, respectively, where 2R and 2S are positive integers; and

a dual-capture match line signal repeater that is configured to isolate the xR and xS match line segments from each other during a first evaluation time interval, pass a match signal from the xR match line segment to the xS match line segment during a first capture time interval and pass a late miss signal from the xR match line segment to the xS match line segment during a second capture time interval that terminates after termination of the first capture time interval.

22. The CAM array of Claim 21, wherein the second capture time interval commences upon termination of the first capture time interval; and wherein said dual-capture match line signal repeater is further configured to block transfer of the match signal from the xR match line segment to the xS match line segment during the second capture time interval.

23. The CAM array of Claim 21, wherein the first and second capture time intervals overlap in time; and wherein said dual-capture match line signal repeater is further configured to block transfer of the match signal from the xR match line segment to the xS match line segment during at least a portion of the second capture time interval.

24. The CAM array of Claim 21, wherein said dual-capture match line signal repeater comprises:

a first inverter having an input electrically connected to the xR match line segment; and

a second inverter having an input electrically coupled to an output of said first inverter and a tri-state output electrically coupled to the xS match line segment, said second inverter responsive to a first evaluation control signal and a first connect control signal.

25. The CAM array of Claim 24, wherein the first evaluation control signal is an active low signal and the first connect control signal is an active high signal.

26. The CAM array of Claim 25, wherein a falling edge of the first evaluation control signal signifies commencement of the first capture time interval; and wherein a rising edge of the first connect control signal signifies commencement of the second capture time interval.

27. The CAM array of Claim 21, further comprising:

a pair of PMOS pull-up transistors electrically connected in series between the xR match line segment and a power supply line, said pair of PMOS pull-up transistors comprising a first PMOS pull-up transistor having a gate terminal that is responsive to a PBIAS signal and a second PMOS pull-up transistor having a gate terminal that is electrically connected to an output of said first inverter.

28. The CAM array of Claim 21, further comprising:

a PMOS precharge transistor having a first current carrying terminal electrically connected to the xR match line segment, a second current carrying terminal electrically coupled to a power supply line and a gate terminal that is responsive to a zeroth evaluation control signal.

29. The CAM array of Claim 28, wherein said dual-capture match line signal repeater comprises:

a first inverter having an input electrically connected to the xR match line segment; and

a second inverter having an input electrically coupled to an output of said first inverter and a tri-state output electrically coupled to the xS match line segment, said second inverter responsive to a first evaluation control signal and a first connect control signal.

30. The CAM array of Claim 21, wherein the first evaluation time interval is synchronized to a zeroth evaluation control signal, the first capture time interval is synchronized to a first evaluation control signal and the second capture time interval is synchronized to a first connect control signal.

31. A content addressable memory (CAM) array, comprising:

a row of CAM cells having at least xR, xS and xT segments of CAM cells therein that include xR, xS and xT match line segments, respectively, where 2R, 2S and 2T are positive integers;

a first dual-capture match line signal repeater that is configured to isolate the xR and xS match line segments from each other during an first evaluation time interval, pass a match signal from the xR match line segment to the xS match line segment during a first early capture time interval and pass a late miss signal from the xR match line segment to the xS match line segment during a first late capture time interval that terminates after termination of the first early capture time interval; and

a second dual-capture match line signal repeater that is configured to isolate the xS and xT match line segments from each other during a second evaluation time interval, pass a match signal from the xS match line segment to the xT match line segment during a zeroth early capture time interval and pass a late miss signal from the xS match line segment to the xT match line segment during a zeroth late capture time interval that terminates after termination of the zeroth early capture time interval.

32. The CAM array of Claim 31, wherein the first late capture time interval and the first early capture time interval do not overlap in time.

33. The CAM array of Claim 31, wherein said first dual-capture match line signal repeater comprises:

a first inverter having an input electrically connected to the xR match line segment; and

a second inverter having an input electrically coupled to an output of said first inverter and a tri-state output electrically coupled to the xS match line segment, said second inverter responsive to a first evaluation control signal and a first connect control signal.

34. The CAM array of Claim 33, wherein said second dual-capture match line signal repeater comprises:

a third inverter having an input electrically connected to the xS match line segment; and

a fourth inverter having an input electrically coupled to an output of said third inverter and a tri-state output electrically coupled to the xT match line segment, said fourth inverter responsive to a zeroth evaluation control signal and a zeroth connect control signal.

35. The CAM array of Claim 34, further comprising:

a PMOS precharge transistor having a first current carrying terminal electrically connected to the xR match line segment, a second current carrying terminal electrically coupled to a power supply line and a gate terminal that is responsive to the zeroth evaluation control signal.

36. A method of searching a CAM array, comprising the steps of:

precharging a first match line segment that is connected to a first segment of CAM cells in a first row of the CAM array; and

performing a staged search operation by:

applying a first segment of a search word to first data lines that are electrically coupled to the first segment of CAM cells while concurrently isolating the first match line segment from a second match line segment that is connected to a second segment of CAM cells in the first row of the CAM array;

passing a match signal from the first match line segment to the second match line segment, during a first capture time interval; and

correcting an erroneous capture of the match signal by passing a late miss signal from the first match line segment to the second match line segment during a second capture time interval that terminates after termination of the first capture time interval.

37. The method of Claim 36, wherein said step of passing a late miss signal is performed concurrently with a step of applying a second segment of the search word to second data lines that are electrically coupled to the second segment of CAM cells.

38. The method of Claim 37, wherein said step of passing a match signal is performed concurrently with a step of globally masking the second data lines.

39. The method of Claim 38, wherein said step of passing a match signal is performed in-sync with a first evaluation control signal; and wherein said step of correcting an erroneous capture is performed in-sync with a first connect control signal.

40. The method of Claim 36, wherein said step of passing a match signal is performed in-sync with a first evaluation control signal; and wherein said step of correcting an erroneous capture is performed in-sync with a first connect control signal.

41. A method of searching a CAM array having first, second, third and fourth segments of CAM cells therein, comprising the steps of:

applying a first segment of a search word to first data lines that are electrically coupled to the first segment of CAM cells while simultaneously applying a third segment of a prior search word to third data lines that are electrically coupled to the third segment of CAM cells;

passing an first match signal from a first match line segment associated with the first segment of CAM cells to a second match line segment associated with the second segment of CAM cells, while concurrently passing a second match signal from a third match line segment associated with the third segment of CAM cells to a fourth match line segment associated with the fourth segment of CAM cells, during a first capture time interval; and

passing a first late miss signal from the first match line segment to the second match line segment and a second late miss signal from the third match line segment to the fourth match line segment, during a second capture time interval that terminates after termination of the first capture time interval.

42. The method of Claim 41, wherein the first and second capture time intervals are nonoverlapping.

43. A content addressable memory (CAM) array, comprising:

a row of CAM cells comprising first and second match line segments; and

a dual-capture match line signal repeater electrically connected to the first and second match line segments, said repeater comprising:

a first inverter having an input electrically coupled to the first match line segment; and

a second inverter having an input electrically coupled to an output of said first inverter and a tri-state output electrically coupled to the second match line segment.

44. The CAM array of Claim 43, wherein said second inverter is responsive to an evaluation control signal and a connect control signal.

45. The CAM array of Claim 44, wherein a pull-up path in said second inverter is enabled when the evaluation control signal is active; and wherein a pull-down path in said second inverter is enabled when the connect control signal is active.

46. The CAM array of Claim 45, wherein the evaluation control signal is an active low signal; and wherein the connect control signal is an active high signal.

47. A content addressable memory (CAM) array, comprising:

a row of CAM cells having at least xR and xS segments of CAM cells therein that include xR and xS match line segments, respectively, where 2R and 2S are positive integers; and

a dual-capture match line signal repeater that is configured to:

transfer a match signal from the xR match line segment to the xS match line segment during an early capture time interval while simultaneously blocking transfer of a miss signal from the xR match line segment to the xS match line segment; and

transfer the miss signal from the xR match line segment to the xS match line segment during a late capture time interval that terminates after termination of the early capture time interval.

48. The CAM array of Claim 47, wherein said dual-capture match line signal repeater is further configured to block transfer of the match signal from the xR match line segment to the xS match line segment during at least a portion of the late capture time interval.

49. The CAM array of Claim 48, wherein the late capture time interval commences upon termination of the early capture time interval.

50. The CAM array of Claim 47, wherein said dual-capture match line signal repeater is further configured to block transfer of the match signal from the xR match line segment to the xS match line segment during the entire late capture time interval.

51. The CAM array of Claim 48, wherein said dual-capture match line signal repeater comprises an inverter having a tri-state output that is electrically connected to the xS match line segment.

52. A method of performing a pipelined search operation within a segmented CAM array, comprising the steps of:

applying a first segment of a search word to first data lines that are electrically coupled to the first segment of CAM cells during a first stage of the pipelined search operation; then

passing a match signal from a first match line segment associated with the first segment of CAM cells to a second match line segment associated with a second segment of CAM cells, while second data lines that are electrically coupled to the second segment of CAM cells are being globally masked; and then

applying a second segment of the search word to the second data lines during a second stage of the pipelined search operation, while simultaneously passing a late miss signal from the first match line segment to the second match line segment to thereby discharge the second match line segment.

53. A method of performing a pipelined search operation within a segmented CAM array, comprising the steps of:

passing an early match signal from a first segment of CAM cells to a second segment of CAM cells during a first stage of a pipelined search operation; and

passing a late miss signal from the first segment of CAM cells to the second segment of CAM cells during a second stage of the pipelined search operation.

54. The method of Claim 53, where said step of passing a late miss signal comprises passing a late miss signal in-sync with applying a second segment of a search word to data lines coupled to the second segment of CAM cells.

55. The method of Claim 54, where said step of passing an early match signal comprises passing an early match signal in-sync with globally masking data lines coupled to the second segment of CAM cells.

56. The method of Claim 53, where said step of passing an early match signal comprises passing an early match signal in-sync with globally masking data lines coupled to the second segment of CAM cells.